ASYNCHRONOUS EXCITERS AND STABILIZERS OF WELDING ARC. ANALYSIS AND DESIGN PROCEDURE. Part 1

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Issues of circuit engineering and analysis of processes in electronic voltage boosters of asynchronous type with series switching-in of main and pilot arcs are considered. They have configuration of forming circuit, in which capacitive storage and inductance of primary winding of pulse step-up transformer have series connection, and switching key of the circuit is switched on in parallel to this connection. The first part of work describes circuit engineering solutions for imbedded asynchronous exciters and stabilizers of arcing process for charging devices based on key scheme with dosing reactor and diode-capacitor voltage multiplier. Analysis of arcing process in circuits of these functional assemblies of asynchronous exciters and stabilizers was performed using equations known in theoretical electric engineering. Engineering procedure of design of main components of charging devices for asynchronous exciters and stabilizers of arcing process as well as recommendations on selection of their element base are proposed based on equation solutions. 28 Ref., 3 Tables, 9 Figures.

Keywords: *arc and plasma welding, initial arc excitation, repeated arc ignitions, electronic arc exciters, spark discharge, series connection, design procedure, recommendations*

In recent years, asynchronous-type devices with series connection of main or pilot arc receive more and more distribution among the electronic voltage boosters, which are called exciters and stabilizers of arc and designed for initiation of stationary arc discharge by means of ionizing of inter-electrode gap due to injection of high-voltage pulses in it. The peculiarities of such devices are:

- consistency of energy and amplitude of output high-voltage pulses independent on periods of connection of switching key of device generator part;
- configuration of forming circuit according to which switching semi-conductor key has in parallel connection to series inductance L and circuit capacity C;
- in number of cases separate circuits of pulse aperiodic charge of capacity C using increased (in relation to device supply voltage) voltage of direct current and charge (recharge) of this capacity, accompanied by transient attenuating process at each connection of forming circuit switching key;
- obviously higher efficiency than in exciters and stabilizers of arc, in which forming circuit represents itself series connection of switching key and reactive elements (L and C);
- possibility of providing of versatility on supply voltage mode (input voltage) in series of cases.

Significant number of works is dedicated to pulse devices, principle of operation of which is based on charge-discharge cycles of capacitive storages of electric energy. Fundamental work [1] provides for the most complete and detailed consideration of theoretical fundamentals of charging circuits of such storages. However, several works, for example [2–4], dedicated to asynchronous exciters and stabilizers of arc (AESA), give piecewise and not enough for practical application consideration to the issues of analysis and electromagnetic processes in the devices of this group, their circuit engineering and calculation. This results in some difficulties in development and designing of AESA.

Aim of the present work lies in consideration and analysis of processes AESA using known theoretical electric engineering methods of investigation of linear circuits and development of recommendations on design and selection of device components of this group, based on results of their analysis and experience of designing, manufacture and practical application.

Peculiarities of circuit engineering, analysis and calculation of AESA functional assemblies. AESA refer to pulse devices providing accumulation of electric energy in periodic mode and its

further consumption through electric discharge for development or retention of plasma.

Capacitive storages are used in AESA for accumulation of electric energy as in number of devices with pulse consumption of energy. Their advantages lie in easy switching of their charging and discharging as well as possibility of controlled dosing of accumulated energy by means of charge voltage level stabilizing [1].

Application of capacitive storages makes for mandatory presence of charging device (CD) in AESA structure. In addition to CD, basic AESA structure includes generator of increased voltage pulses (GVP) with regulation scheme and device for input of high-voltage pulses (DIHVP) in circuit of main or pilot arcs (Figure 1).

Variety of existing at present time engineering solutions of CD and processes taking place in them give grounds to assume that the following can be used for desining of CD in AESA:

- pulse transformation of direct current voltage with the help of semiconductor inverters, DC–DC converters of step-up type, converters based on Polikarpov scheme (often called Cook's scheme), Luo-converters, key schemes with dosing reactors;
- rectification and increase (multiplication) of input voltage of single-phase alternating current to required level of charge voltage of GVP capacitive storage with the help of devices, which are made based on scheme of diode-capacitor voltage multipliers, for example, by Cockcroft –Walton scheme;
- method of resonance pumping.

Processes in CD with inverters are studied in works [1, 5, 6 etc.), analysis and basics of calculation of semiconductor DC–DC converters and converters based on Polikarpov (Cook's) scheme are given in works [5–8] and Luo-converters — in [9]. The most important and general topological indication of all without exception pulse converters of direct current is presence in their structure of one or several inductive storage units as well as regulated semiconductor keys and their controllers, providing formation of control signals of pulse-width or pulse-frequency modulation considering feedback signals on output voltage or current. This provokes for specific engineering difficulty of such converters and application of significant number of necessary components, that inevitably effect safety and cost of CD and AESA in whole.

CD based on key schemes with dosing reactors. CDs based on key schemes with dosing reactors are the simplest ones and have the smallest quantity of elements and, respectively, the lowest cost among known semiconductor pulse converters of direct current voltage. It should be noted that one of the advantages of such CDs lies in constant amount of consumed energy under conditions of providing complete discharge of dosing reactors [1].

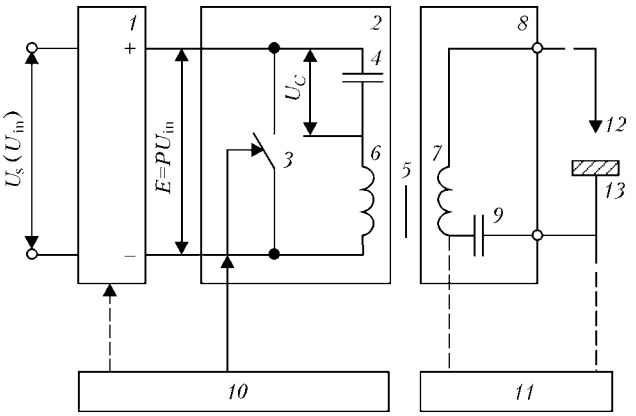

Figure 1. Structural diagram of AESA: *1* — CD of step-up type; *2* — GVP; *3* — semiconductor switching key included in GVP; *4* — capacitor of GVP forming circuit; *5* — pulse step-up transformer with primary winding *6* and secondary winding *7*; *8* — DIHVP in arc circuit; *9* — protective (bypass) capacitor of DIHVP; *10* — AESA control scheme; *11* — arc supply source; *12* — electrode; *13* — part to be welded

Somewhat simplified electric schematic diagram of AESA with CD, which is built based on key scheme with dosing reactor, is given in Figure 2, *a*. Charge of capacitive storage in such CD (condenser *C*2) of GVP forming circuit is carried out for several two-phase cycles of switching of transistor key *VT*1.

Accumulation of energy in inductive storage (choke) *L*1 takes place during the first stage of each cycle, in course of which transistor key *VT*1 is in open (on) condition. Scheme of CD replacement for this stage of its operation is given in Figure 2, *b*. Building up of current i_L through reactor (choke) *L*1 and current i_T through transistor key *VT*1 take place from zero to amplitude value I_m, and process of charging of choke *L*1 at current i_L and voltage u_L are described by equations [10], solutions of which are

$$i_L = i_T = \frac{U_{\text{in}}}{R}\left(1 - e^{-\frac{R}{L}t}\right), \quad u_L = U_{\text{in}} e^{-\frac{R}{L}t}, \qquad (1)$$

where U_{in} is the direct current power voltage (voltage at *C*1 capacitor); $R = R_L + ESR_{C1} + R_{\text{c.e}} + R_{\text{add}}$ is the pure resistance of choke charge circuit *L*1; R_L is the choke pure resistance; ESR_{C1} is the equivalent active series resistance of capacitor *C*1; $R_{\text{c.e}}$ is the pure resistance of collector-emitter of *VT*1 transistor in on condition; R_{add} is the pure resistance of additional current-limiting resistor (*R*2); *L* is the reactor (choke) inductance *L*1.

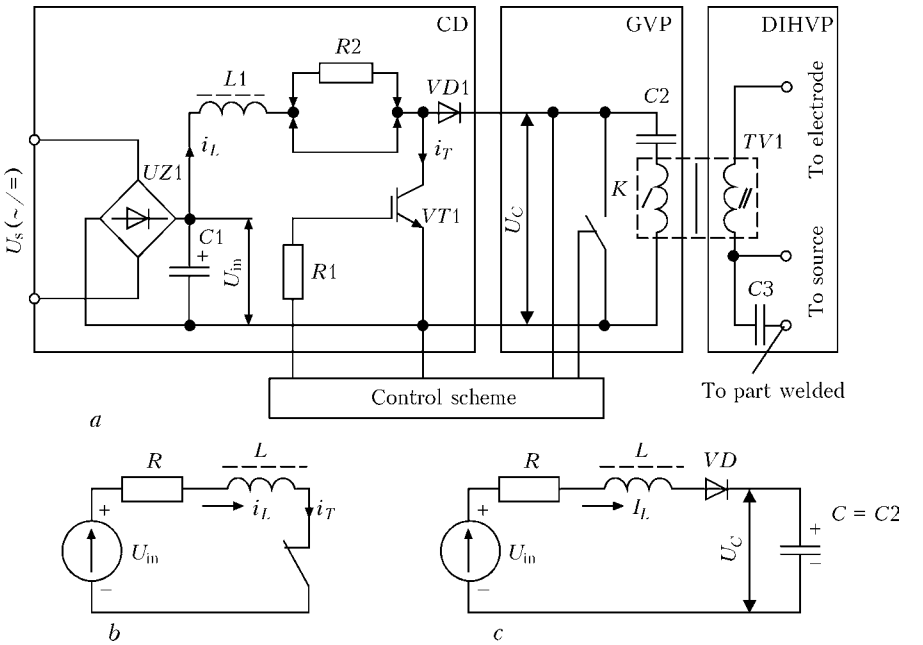

Figure 2. Electrical schematic diagram of AESA with CD based on key scheme with dosing reactor (*a*) and schemes of CD replacement for time interval, corresponding to duration of on- (*b*) and off- (*c*) condition of CD transistor key

Necessity of introduction of additional current-limiting resistor R_{add} (Figure 2, *a*, *R*2) lies in the fact that its presence provides for stability of consumed power for the first moment of charge of capacitive storage (capacitor *C*2). Besides, as long as values of R_L and differential diode resistance *VD*1 in its on condition (conductivity condition) are very small, then it is impossible to provide limitation of charge current of capacitive storage of GVP forming circuit in considered AESA scheme by means of influence on control inlet of transistor key *VT*1. Moreover, it is obvious that introduction of additional current-limiting resistor R_{add} somewhat deteriorates CD energy indices.

The largest (amplitude) value of current I_m, which is achieved in passing of current $i_L = i_T$ in time interval, corresponding to on condition of CD transistor key, is determined by relationship

$$I_m = \frac{U_{in} D}{L f_{t.k}}, \qquad (2)$$

where *D* is the relative duration of on condition of CD transistor key during $T_{t.k}$ of each switching cycle; $f_{t.k} = 1/T_{t.k}$ is the frequency of switching cycles of CD transistor key.

Transistor key *VT*1 (Figure 2, *a*) is transformed in off condition at the beginning of second stage of each cycle, and dose of energy accumulated in inductive storage *L*1 is

$$\Delta W = \int_0^{\tau_a} (u_L i_L) dt = L I_m^2 / 2 = \text{const}, \qquad (3)$$

where τ_a is the pulse duration, in course of which choke *L*1 accumulates energy and this energy starts proceeding in GVP capacitive storage (capacitor *C*2). Scheme of CD replacement for the second stage of charging-discharging cycle of inductive storage *L* is given in Figure 2, *c*.

Below condition, grounded in work [1], is applied to CD transistor key switching frequency $f_{t.k}$ for accumulation of energy on inductive storage *L* and its complete discharge during the second stage of each cycle:

$$f_{t.k} \le \frac{1}{1.57\sqrt{LC} + L I_m / U_{in}}, \qquad (4)$$

where *C* is the capacitor (capacitive storage) capacity of GVP forming circuit.

Considering the fact that AESA as a rule, in addition to value of pulse energy, includes set values of charge voltage U_{C0} of GVP capacitive storage (Figure 2, *a*, *C*2) and duration of its charge t_{ch}, which should fulfill the condition

$$t_{ch} \le \frac{1}{f_{sw}}, \qquad (5)$$

then energy value W_C, accumulation of which should be provided for t_{ch} time interval, makes

$$W_C = \frac{C U_{C0}^2}{2} = n \Delta W = \frac{L I_m^2}{2} t_{ch} f_{t.k}, \qquad (6)$$

where f_{sw} is the frequency of connection of GVP switching key (Figure 2, *a*, *K*); $n = t_{ch}/T_{t.k} = t_{ch} f_{t.k}$ is the amount of cycles of CD transistor key switching (Figure 2, *a*, *VT*1) for t_{ch} time interval.

Solutions of known equations with non-zero initial conditions [10, 11] for replacement

scheme, given in Figure 2, *c*, show that u_L voltage at the storage in the second part of cycle in course of complete discharge τ_d *n*th CD inductive storage in the moment of *n*th pulse beginning is determined as

$$-u_L = -(U_{C_{n-1}} + U_{in}), \quad (7)$$

where $U_{C\,n-1}$ is the GVP capacitive storage voltage before *n*th pulse beginning, and in the moment of *n*th pulse ending the following formula is used:

$$-u_L = -(U_{C_{n-1}} + U_{in})/e^{-\frac{R}{L}\tau_d}. \quad (8)$$

According to work [1] $U_{C_{n-1}}$ voltage can be determined by expression

$$U_{C_{n-1}} = \sqrt{\frac{L}{C(n-1)}}, \quad (9)$$

momentary value of charge current i_C of GVP capacitive storage for *n*th pulse is determined by formulae

$$i_C(\tau)_n = I_m(cos\ \omega_0\tau - \sqrt{n-1}\ \sin\ \omega_0\tau), \quad (10)$$

and τ_d duration — by expression

$$\tau_d = \sqrt{LC}\,(1.57 - \text{arctg}\ \sqrt{n-1}). \quad (11)$$

Here τ is the time taken from the moment of *n*th pulse beginning; $\omega_0 = 1/\sqrt{L\,C}$ is the own frequency of *LRC*-circuit of charge of GVP capacitive storage.

Figure 3 shows diagrams of i_L and i_{VT} currents, passing through inductive storage and CD transistor key, respectively, charge current i_C of GVP capacitive storage (i_{VD} current passing through gate-type diode) and u_C voltage at this storage. It follows from expressions (7)–(11) and Figure 3 that increase of u_C voltage at GVP capacitive storage provides for gradual reduction of τ_d duration of pulses of charge current i_C and $\Delta U_C = U_{C_n} - U_{C_{n-1}}$ voltage difference. Processes of energy accumulation in CD inductive storage and its complete discharge, repeating with $f_{t.k}$ frequency, take place up to the moment of GVP capacitive storage voltage reaching set U_{C0} value, after which discharge (re-charging) of the latter without switching off of its charge circuit is performed in GVP. In order to prevent charging of GVP capacitive storage to U_C voltage values, exceeding allowable ones, it is necessary to switch off supply voltage or U_{in} voltage at the moment of stop of AESA output pulse generation.

Active value of current I_c, consumed by such AESA, for CD scheme, given in Figure 2, *a*, can be determined by relationship

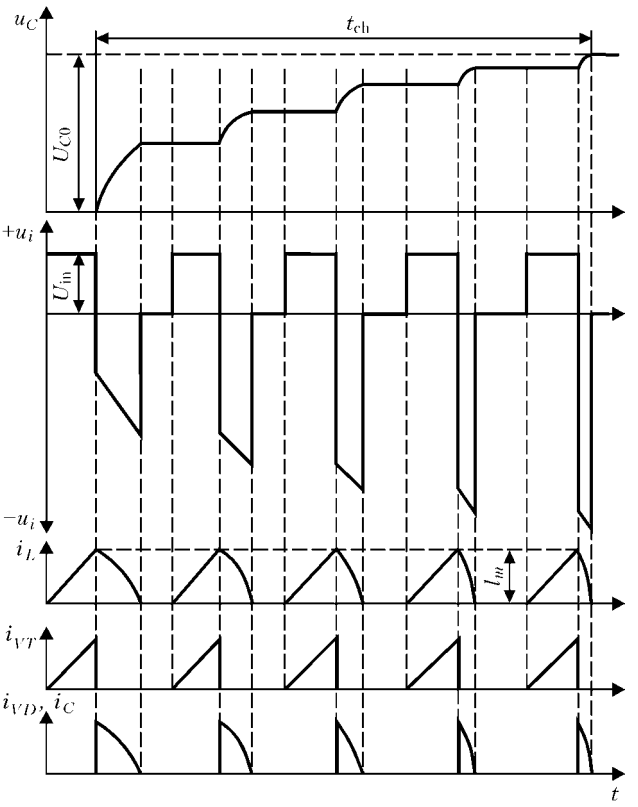

Figure 3. Diagrams of voltages and currents in CD circuits based on key scheme with dosing reactor

$$I_c = \frac{U_{in}}{4.9Lf_{t.k}}, \quad (12)$$

and amplitude value of current I_m necessary for charging of GVP capacitive storage (at set values of U_{C0} and t_{ch}) — by expression

$$I_m = \sqrt{\frac{C}{L\,t_{ch}f_{t.k}}}\,U_{C0} = \sqrt{\frac{C}{Ln}}\,U_{C0}. \quad (13)$$

Advantages of CD, constructed on key scheme with dosing reactor (see Figure 2, *a*), are practical absence of limitations on the level of input voltage U_{in} (making in most cases from 50 to 350 V) as well as invariance of such CD by kind of AESA supply voltage. At that standard functioning of CD in AESA supplied by alternating current voltage does not depend on its frequency. If only direct current voltage is provided for AESA supply, then presence of *UZ*1 rectifier and *C*1 buffer capacitor in the scheme, given in Figure 2, *a*, is not mandatory.

However, practice shows that CDs based on key scheme with dosing reactor have some limitations on the level of complete charge voltage U_{C0} of GVP capacitive storage. This is provoked by the fact that rise of U_{C0} inevitably determines and tightens the requirements on maximum allowable values of transistor key *VT*1 collector-emitter ($U_{c.e\ max}$) voltage (see Figure 2, *a*) and voltage on switching key *K* of GVP forming cir-

Table 1. Calculation value of pulse stored energy (J) depending on capacity of GVP forming circuit

C_{C0}, V	C, μF										
	0.05	0.10	0.15	0.20	0.25	0.30	0.40	0.50	0.60	0.70	0.80
600	0.278	0.556	0.833	1.111	1.389	1.667	2.222	2.778	3.333	3.889	4.444
650	0.237	0.473	0.710	0.997	1.183	1.420	1.893	2.367	2.840	3.314	3.787
700	0.204	0.408	0.612	0.816	1.020	1.224	1.633	2.041	2.449	2.857	3.265
750	0.178	0.356	0.533	0.711	0.889	1.067	1.422	1.778	2.133	2.489	2.844
800	0.156	0.313	0.469	0.625	0.781	0.938	1.250	1.563	1.875	2.188	2.500

cuit in off condition of these keys, back voltage of diode $VD1$ and voltages on AESA passive elements. Regardless the basic possibility of achievement of high levels of U_{C0}, its recommended values make from 600 to 800 V based on experience of development and application of AESA, available range of key semiconductor devices and their costs.

Engineering calculation of basic components of CD, constructed on the basis of key scheme with dosing reactor at set value of stored energy of W_C pulses, U_{in} and U_{C0} voltages, frequency f_{sw} or $T_{\text{sw}} = (f_{\text{sw}} = 1/T_{\text{sw}})$ period of connection of GVP switching key can be carried out in the following way:

1. Minimum necessary value of capacity C of GVP forming circuit (see Figure 2, *a*, $C2$) is determined with the help of relationship (6) and values, given in Table 1:

$$C \geq \frac{2W_C}{U_{C0}^2}. \qquad (14)$$

In accordance to the earlier carried investigations and obtained experimental data the recommended values of pulse stored energy W_C depending on AESA value are 0.05–0.50 J for arc exciters and that for pulse stabilization of process of burning of alternating current arc make 0.20 and 0.80 J [2, 3, 12].

The closest value (with rounding to larger side) from 0.10, 0.15, 0.22, 0.33, 0.47, 0.68, 1.00, 1.50 μF series is taken as calculation value of capacitor capacity $C2$ (see Figure 2, *a*) based on determined according to (14) or Table 1. At that necessary C value can be received due to dissipative (parallel) switching of two-four capacitors with polyethylene or polycarbonate dielectric, characteristics and parameters of which correspond to the recommendations, given in [13] (for example, capacitors of PPA or PPB series of ICEL company).

2. The value of figure n is taken according to condition (4) and depending on values of frequency f_{sw} or $T_{\text{sw}}(f_{\text{sw}} = 1/T_{\text{sw}})$ period of connection of GVP switching key (frequency or period of passing of AESA output pulses) and energy of W_C pulses. This figure based on expression (7) determines number of ΔW_C energy doses, accumulation of which provide for complete charge of GVP capacitive storage to U_{C0} level for t_{ch} time interval. Table 2 shows recommended values of n.

3. Amplitude value of I_m current passing through reactor and relative duration D of on condition of CD transistor key are determined based on expressions (2), (5) and (6) and figure $n = W_C/W_C = t_{\text{ch}}/T_{\text{t.k}} = t_{\text{ch}}f_{\text{t.k}}$ taken according to Table 2. Recommended I_m values following the results of carried investigations and experimental data and depending on set values of W_C, W_{in} or U_{C0}; f_{ch} make from 2.2 to 3.2 A and D value is from 0.24 to 0.30. At that values being selected in indicated ranges of I_m and D should increase with rise of U_{in} values or decrease of n figure values.

4. L is determined by expression below assuming that inductance of dosing reactor $L1$ (see Figure 2, *a*) is linear and does not depend on current i_L passing through reactor, and using calculated and selected values of I_m, n and D as well as set U_{in} and W_C values considering (2)

Table 2. Recommended n values depending on f_{sw} and W_C

f_{sw}, Hz	W_C, J										
	0.05	0.10	0.15	0.20	0.25	0.30	0.40	0.50	0.60	0.70	0.80
From 50 to 100	1	2	3	4	5	6	8	8	9	10	10
Over 100 to 120	1	2	3	4	5	6	6; 7	8	8	8	8
Over 120 to 200	1	2	2	3	3	3; 4	4; 5	5	5	5	5

$$L = \frac{U_{\text{in}} D}{I_m^2 f_{\text{t.k}}}, \quad (15)$$

and considering (6)

$$L = \frac{2W_C}{I_m^2 n}. \quad (16)$$

Diagrams of $L = f(U_{\text{in}}, I_m, D, f_{\text{t.k}})$ dependence is illustrated by Figure 4.

Figure 5 gives the recommended values of dosing reactor inductance $L1$, following from Table 2, range of I_m recommended values, expressions (15) and (16) as well as experience of development and application of AESA CD based on key scheme with dosing reactor.

Many works, for example [14–17], are dedicated to theoretical fundamentals, analysis of processes and procedures of electromagnetic calculations and design of inductive elements with ferromagnetic cores, including chokes of ultra-low, low and average frequencies. These works indicate that shell-type structure is the most efficient for CD dosing reactor on the basis of electromagnetic and weight-dimension indices. Such a structure can be built on the basis of cores from E-type plates or strip magnetic conductors from sheet cold-rolled anisotropic electrical steel of 3411–3412 grades. At that, length of total diamagnetic gap in a core of dosing reactor should make 1.05–1.50 mm.

5. After inductance of dosing reactor $L1$ is determined, it is necessary to specify calculation amplitude value of current I_m. Expressions (2) or (13) can be used for this.

6. Determining resistance R of $R2$ resistor (see Figure 2, *a*) requires consideration of the next facts, namely, first of all, since $R_{\text{add}} >> R_L + ESR_{C1} + R_{T0}$, then $R \approx R_{\text{add}}$ and, for the second, obtaining of linear dependence $i_L = f(t)$ through application of initial (virtually linear) part of exponent during charging of dosing reactor $L1$ necessitates fulfilment of condition

$$L/R > \tau_{\text{ch}}. \quad (17)$$

Recommended values of $R2$ resistor resistance make from 6 to 22 Ohm assuming that $L/R >> 1/f_{\text{sw}}$ and considering results of calculation, experimental data and recommended values of $f_{\text{t.k}}$, I_m, U_{C0} and L. They increase with rise of U_{in} values or reduction of $f_{\text{t.k}}$ values.

Lager value of dissipation power $P_{R2\,\max}$, emitted in resistor $R2$ during two first cycles of charging-discharging of dosing reactor $L1$, can be determined by expression

$$P_{R2\,\max} = I_{\text{c.a}}^2 R2 = I_m^2 D R2, \quad (18)$$

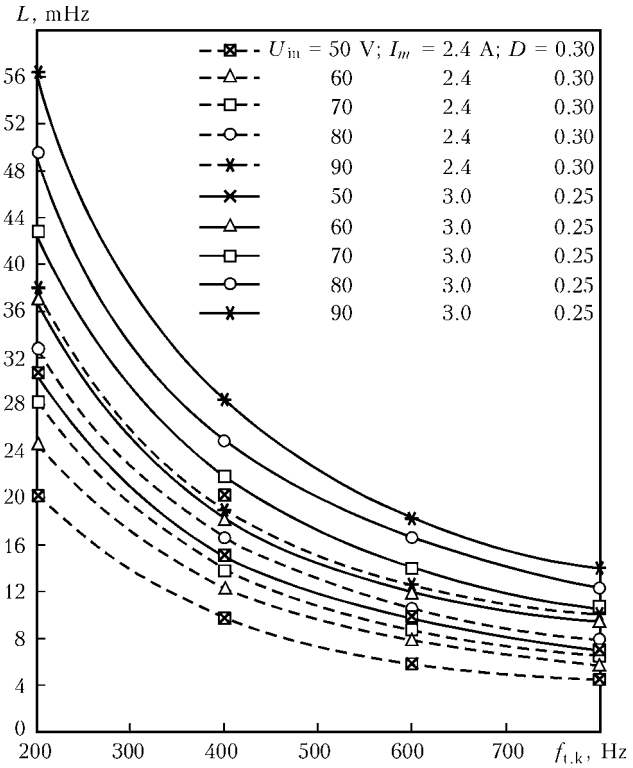

Figure 4. Diagrams of dependence of dosing reactor inductance $L = f(U_{\text{in}}, I_m, D, f_{\text{t.k}})$

where $I_{\text{c.a}} = I_c/\sqrt{1/D}$ is the active value of current i_L, passing through resistor $R2$. Since rise of U_C (see Figure 3) provides for reduction of discharge current of dosing reactor $L1$ in each next cycle, then up to the moment of ending of GVP capacitive storage charge the power $P_{R2\,\min}$ emitted in resistor $R2$ is determined as

$$P_{R2\,\min} \approx 0.5 I_m^2 D R2. \quad (19)$$

It follows from (18) and (19) that average value of power P_{R2}, emitted in resistor $R2$, is

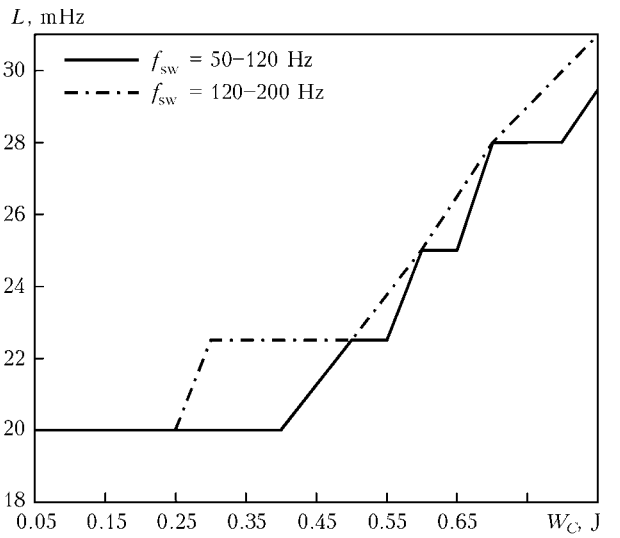

Figure 5. Recommended values of choke inductance of CD based on key scheme with dosing reactor at U_{C0} = (700 ± ± 100) V

$$P_{R2} \approx 0.75 I_m^2 DR2. \quad (20)$$

If AESA is designed for stabilizing of process of alternating current arc burning, then nominal power $P_{R2\,\text{nom}}$ of resistor $R2$ is taken from condition

$$P_{R2\,\text{nom}} \geq 1.67 P_{R2} \quad (21)$$

in the case of AESA application only for initial excitation of direct current arc, the value of nominal power of resistor $R2$ can be significantly reduced in comparison with the value, calculated according to (21), and should make 6–10 W.

Power resistors of C5–C35 series or SPS, SQZ, SQHG [18] series are good to be used as $R2$ resistor.

7. Maximum value of voltage of collector-emitter is $U_{\text{c.e}} \approx U_{C0}$, and maximum value of current of collector makes $I_{\text{c}} \approx I_m$ during selection of CD transistor key (see Figure 2, *a*, *VT*1), proceeding from the fact that according to (5) and Table 2 switching frequency $f_{\text{t.k}}$ of this key does not exceed 1000 Hz. It can be assumed based on this that the most appropriate for application as CD transistor key are IGBT-transistors, which have

$$U_{\text{c.e max}} \geq 1.2 U_{C0}, \quad I_{\text{c max}} \geq 1.5 I_m, \quad I_{\text{c, p max}} \geq 1.15 (U_{\text{in}}/R), \quad (22)$$

where $U_{\text{c.e max}}$ is the maximum allowable voltage of collector-emitter in off condition; $I_{\text{c max}}$ and $I_{\text{c, p max}}$ are, respectively, the maximum allowable direct and pulse current of collector in on condition. Taking into account (22) IRG4BH20K, IRG4PN30R, IRG4PH40KD IGBT-transistors and similar to them of «International Rectifier» [19] or IGW08T120 of «Infineon» companies can be recommend as example for application in CD key, at that resistor resistance $R1$ (see Figure 2, *a*) in gate circuit of such transistors should make 8–12 Ohm.

8. The main parameters for selection of diode $VD1$ (see Figure 2, *a*) are maximum allowable values of average direct current I_F and back voltage U_R as well as maximum value of forward drop U_F and time of reverse recovery t_{rr}. At that, parameters of diode $VD1$ should fulfill the conditions

$$U_{R\,\text{max}} \geq 1.2 U_{C0}, \quad I_{F\,\text{max}} \geq 1.2 I_{\text{av. max}}, \quad (23)$$

where $I_{\text{av. max}}$ is the maximum average value of charge current of GVP capacitive storage, which can be determined with the help of expression

$$I_{\text{av.max}} = 0.5 I_{\text{a.c}}. \quad (24)$$

Diode BYV26E of Vishay Semiconductors Company [20] can be used, for example, in CD according to combination of parameters and characteristics.

CD based on diode-capacitor voltage multipliers. In comparison with earlier considered the CDs based on voltage multiplies (VM) are characterized by absence of inductive and controlled semi-conductor elements, significantly lower values of weight-dimension indices, and, respectively, higher specific power as well as significantly lower cost. Regardless the fact that VMs have been already known from the 30th of the last century and are still used in television and medical equipment, measurement equipment, night vision equipment and many other fields of engineering [21], this class of devices is not studied enough, and works, dedicated to analysis and procedure of VM design, are not numerous. For example, [22, 23] mainly reflect aspects of VM work with supply from sine-wave voltage sources of commercial frequency. At the same time, there is a tendency in recent decade to intensive development of investigations and designs as well as spread of VM application with high frequency pulse supply from inverters operating in switching mode. Series of last works, for example [6, 24–26], provide for sufficiently strict and detailed considerations and analysis of aspects of circuit engineering, transition processes and dynamic characteristics of such VM. Taking into account mentioned above, present work will be restricted by issues of design and selection of VM elements being used in AESA CD construction, in particular, for providing of initial and repeated arc excitations in inverters for nonconsumable-electrode inert-gas (TIG) welding, for example, in Master Tig 2500, Master Tig 3500 and other models of KEMPPI company [27].

Devices, built by Cockcroft–Walton scheme (scheme of asymmetric single-phase half-wave VM), were the most widespread among the known diode-capacitor VM in AESA. Simplicity of this scheme realizing and possibility of its application at any stage (of cascades) of voltage multipliers with direct current operating voltage, not exceeding peak-to-peak value of direct current input voltage (AESA supply voltage) can be refereed to its advantages. Among the disadvantages are limited load-carrying capacity due to dropping external volt-ampere characteristic typical for all diode-capacitor VM (and, respectively, significant output resistance) and voltage drop in VM depending on voltage current and number of multiplying stages, high sensitivity to oscillations of values of input current and its frequency as well as fundamental necessity in exclusive application of alternating current voltage of sine-wave and rectangular-wave forms as input one.

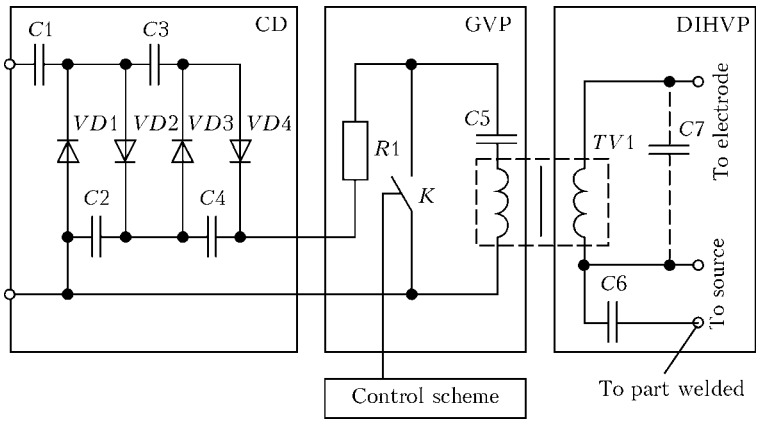

Figure 6. Typical electric schematic diagram of AESA with CD based on VM built on four-stage Cockcroft–Walton scheme

The following was determined as a result of carried investigations of VM based on Cockcroft–Walton scheme [23–26], namely values of direct current output voltage U_{out} virtually do not depend on form of alternating current input voltage; VM characteristics are improved with increase of input voltage frequency f_{in}, values of which should be in the limits of 5–50 kHz, at that the most optimum values are 15–40 kHz; VM power for providing acceptable characteristics of its load-carrying capacity should be not lower than 50 W and multiplication factor (number of multiplication stages N) makes from 3 to 6; rectangular-wave input voltage is the most heavy current operation mode for diodes in VM cascades, therefore, their designing requires stipulation of measures for limitation of diode starting current.

Example of typical fundamental electric scheme of AESA, CD of which is built based on four-cascade VM and performed by Cockcroft–Walton scheme, is given in Figure 6.

Capacitor $C1$ will charge to amplitude value of this voltage $U_{in.m}$ during negative half-wave of input voltage through open diode $VD1$. Capacitor $C2$ will charge to $2U_{in.m}$ level during positive half-wave after negative one through open diode $VD2$, and capacitor $C3$ will charge to $2U_{in.m}$ level in course of following after this negative half-wave through open diode $VD3$, and capacitor $C4$ will charge to $2U_{in.m}$ level in the next positive half-period of input voltage through open diode $VD4$. Thus, direct current input voltage in VM open-circuit mode represents itself sum of voltages based on series and stationary re-charging capacitors $C2$ and $C4$ and makes $4U_{in.m}$. According to [21–26] the output voltage U_{out} in load mode under condition of time stability of values of input voltage $U_{in.m}$ and its frequency f_{in} is determined by formulae

$$U_{out} = NU_{in.m} - \frac{I_{l.c}(N^3 + 9N^2/4 + N/2)}{12f_{in}C_{st}}, \quad (25)$$

where $I_{l.c}$ is the largest value of VM load current; C_{st} is the capacitor capacity of each stage of multiplication under $C_{st} = C1 = C2 = C3 = C4$ condition. Formulae (25) at $N = 4$ (see Figure 6) can be represented as

$$U_{out} = 4U_{in.m} - \frac{8.5I_{l.c}}{f_{in}C_{st}}. \quad (26)$$

Deduction in expression (25) and (26) is a drop of voltage $\Delta U = r_{out}I_{l.c}$ of multiplier, from which value of output resistance r_{out} can be determined by expression

$$r_{out} = \frac{N^3 + 9N^2/4 + N/2}{12f_{in}C_{st}}, \quad (27)$$

and at $N = 4$

$$r_{out} = \frac{8.5}{f_{in}C_{st}}. \quad (28)$$

Considering that $f_{in} >> f_{sw}$ and charge of GVP capacitive storage (Figure 6, $C5$) is performed for number of full cycles of formation of multiplier output voltage U_{out}, it can be assumed that to a first approximation $i_C(t)$ current and $u_C(t)$ voltage of charge of capacitive storage in course of this charge duration $\tau_{ch} \approx 1/f_{sw}$ are changed by expressions [10]

$$i_C(t) = I_m e^{-\frac{t}{RC}}, \quad u_C(t) = U_{out}\left(1 - e^{-\frac{t}{RC}}\right). \quad (29)$$

Here the largest (amplitude) I_{amp} value of charge current $i_C(t)$ corresponds to charge initial moment $t = 0$ (in which $u_C(t) = 0$); $R = R_{lim} + ESR_C + R_{L1} \approx R_{lim}$ is the sum of pure resistances of current-limiting resistor $R1$ (see Figure 6), equivalent series resistance of capacitor (capacitive storage), forming GVP circuit and pure resistance of primary winding of pulse transformer

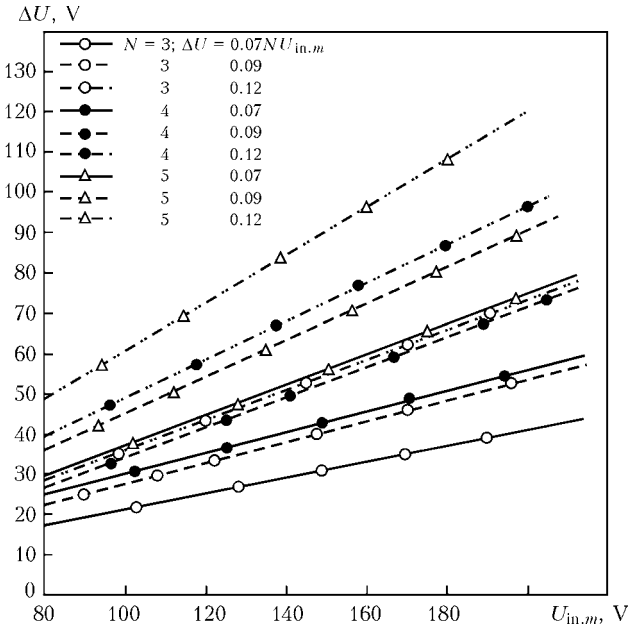

Figure 7. Diagrams of dependence of voltage drop $\Delta U = f(N, U_{\text{in}.m})$ in VM built by Cockcroft–Walton scheme

*TV*1. When charging of GVP capacitive storage by voltage formed with the help of VM, current of its charge $i_C(t)$ is reduced with increase of $u_C(t)$ voltage in this storage, the same as in variant of CD based on key scheme with dosing reactor. Therefore, $I_{\text{l.c}} = I_m = \Delta U / r_{\text{out}} = NU_{\text{in}.m} / r_{\text{out}} + R_{\text{lim}}$ value is the maximum and typical only for the first cycle of charge of GVP capacitive storage, and ΔU voltage drop is reduced synchronously with charge current $i_C(t)$ reduction.

If $\Delta U = (0.07–0.10)NU_{\text{in}.m}$ is set, that can be fulfilled in practice, as shown by calculation and measurement results (diagrams of dependence

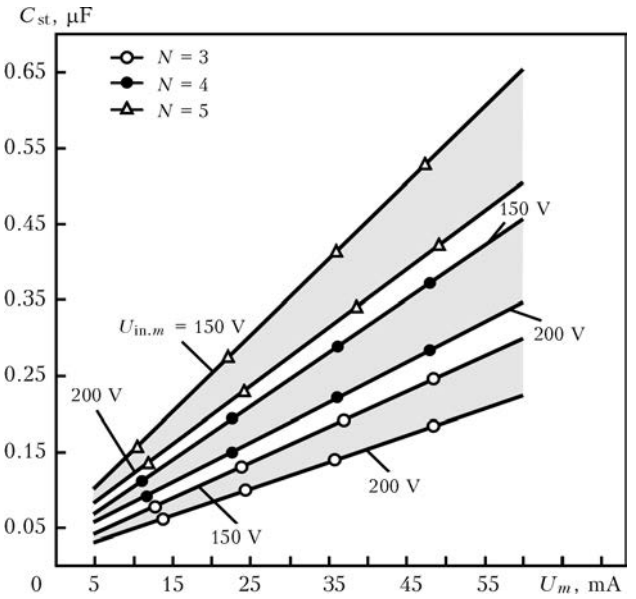

Figure 8. Dependence diagrams of $C_{\text{st}} = f(I_{\text{amp}}, U_{\text{in}.m}, N)$ capacity of each stage of VM at $f_{\text{in}} = 20$ kHz and $\Delta U = 0.01NU_{\text{in}.m}$

$\Delta U = f(N, U_{\text{in}.m})$ are given in Figure 7), then I_m according to (25) and (27) can be determined by formulae

$$I_m = \frac{(0.07–0.10)NU_{\text{in}.m}12f_{\text{in}}C_{\text{st}}}{N^3 + 9N^2/4 + N/2}, \qquad (30)$$

and C_{st} — by formulae

$$C_{\text{st}} = \frac{I_{\text{amp}}(N^3 + 9N^2/4 + N/2)}{(0.07–0.10)NU_{\text{in}.m}12f_{\text{in}}}. \qquad (31)$$

$C_{\text{st}} = f(I_m, U_{\text{in}.m})$ dependence diagrams at $\Delta U = 0.1NU_{\text{in}.m}$ and $f_{\text{in}} = 20$ kHz are given in Figure 8, and $C_{\text{st}} = f(f_{\text{in}}, I_m)$ dependence diagrams at $\Delta U = 0.1NU_{\text{in}.m}$ and $N = 4 \div 5$ — in Figure 9.

In the case of sine-wave input voltage of VM (AESA supply voltage) and assuming that pure resistance of capacitor charge circuit of each VM stage is negligibly small, the largest (peak) value of I_{FSM} and the largest average I_{FAV} value of direct current through diode of this multiplying stage can be determined with accuracy sufficient for practice as

$$I_{FSM} = 12.56\,U_{\text{in}.m}f_{\text{in}}C_{\text{st}}, \quad I_{FAV} = 0.318\,I_{FSM}, \qquad (32)$$

I_{FSM} parameter in the case of rectangular VM input voltage can be determined based on the fact that $i_{C_{\text{st}}} = d\,U_{C_{\text{st}}}/dt$. Considering that $dt = \tau_{\text{f}}$ (where τ_{f} is the duration of growth of front for VM input peak-to-peak voltage), and assuming $\tau_{\text{f}} = 0.04T_{\text{in}}$ (that is typical for most welding inverters), I_{FSM} and I_{FAV} values can be determined as

$$I_{FSM} = 100\,U_{\text{in}.m}f_{\text{in}}C_{\text{st}}. \quad I_{FAV} = U_{\text{in}.m}f_{\text{in}}C_{\text{st}}, \qquad (33)$$

It was experimentally determined that the following condition should be fulfilled in use of VM in each cycle of charge of GVP capacitive storage:

$$0.5NT_{\text{in}} < \tau_{\text{ch}} < 0.9T_{\text{sw}}, \qquad (34)$$

where $\tau_{\text{ch}} = (R_{\text{lim}} + r_{\text{out}})C = R_{\text{ch}}C$, from which

$$R_{\text{ch}} \le 0.9T_{\text{sw}}/C. \qquad (35)$$

Based on (27) and (35) resistance of current-limiting resistor R_{lim} (see Figure 6, $R1$) can be determined by formulae

$$R_{\text{lim}} \le \frac{0.9T_{\text{sw}}}{C} - \frac{N^3 + 9N^2/4 + N/2}{12f_{\text{in}}C_{\text{st}}}. \qquad (36)$$

Calculation of VM-based CD, built by Cockcroft–Walton scheme, at set values of pulse energy W_C, frequency f_{in} or period T_{in} of input voltage $U_{\text{in}}(f_{\text{in}} = 1/T_{\text{in}})$ and frequency f_{sw} or period T_{sw} of connection of GVP switching key ($f_{\text{sw}} = 1/T_{\text{sw}}$), is carried out in the following way:

Table 3. Calculation values of I_m and R_{ch} for VM-based CD

f_{sw}, Hz	$0.9T_{sw}\cdot10^2$, s	U_{out}, V	C, μF	R_{ch}, kOhm	I_m, A
50	1.80	600	0.5–1.5	12	0.050
			1.5–2.0	9	0.056
			3.0	6	0.100
			4.0	4.5	0.133
		650	0.5–1.5	12	0.054
			1.5–2.0	9	0.062
			3.0	6	0.108
			4.0	4.5	0.144
		700	0.5–1.5	12	0.058
			1.5–2.0	9	0.066
			3.0	6	0.117
			4.0	4.5	0.177
100	0.90	600	0.5–1.5	9	0.056
			1.5–2.0	4.5	0.133
			3.0	3	0.200
			4.0	2.25	0.266
		650	0.5–1.5	9	0.062
			1.5–2.0	4.5	0.144
			3.0	3	0.217
			4.0	2.25	0.290
		700	0.5–1.5	9	0.066
			1.5–2.0	4.5	0.156
			3.0	3	0.233
			4.0	2.25	0.311
200	0.45	600	0.5–1.5	12	0.133
			1.5–2.0	9	0.266
			3.0	6	0.400
			4.0	4.5	0.530
		650	0.5–1.5	12	0.144
			1.5–2.0	9	0.290
			3.0	6	0.433
			4.0	4.5	0.575
		700	0.5–1.5	12	0.156
			1.5–2.0	9	0.311
			3.0	6	0.467
			4.0	4.5	0.620

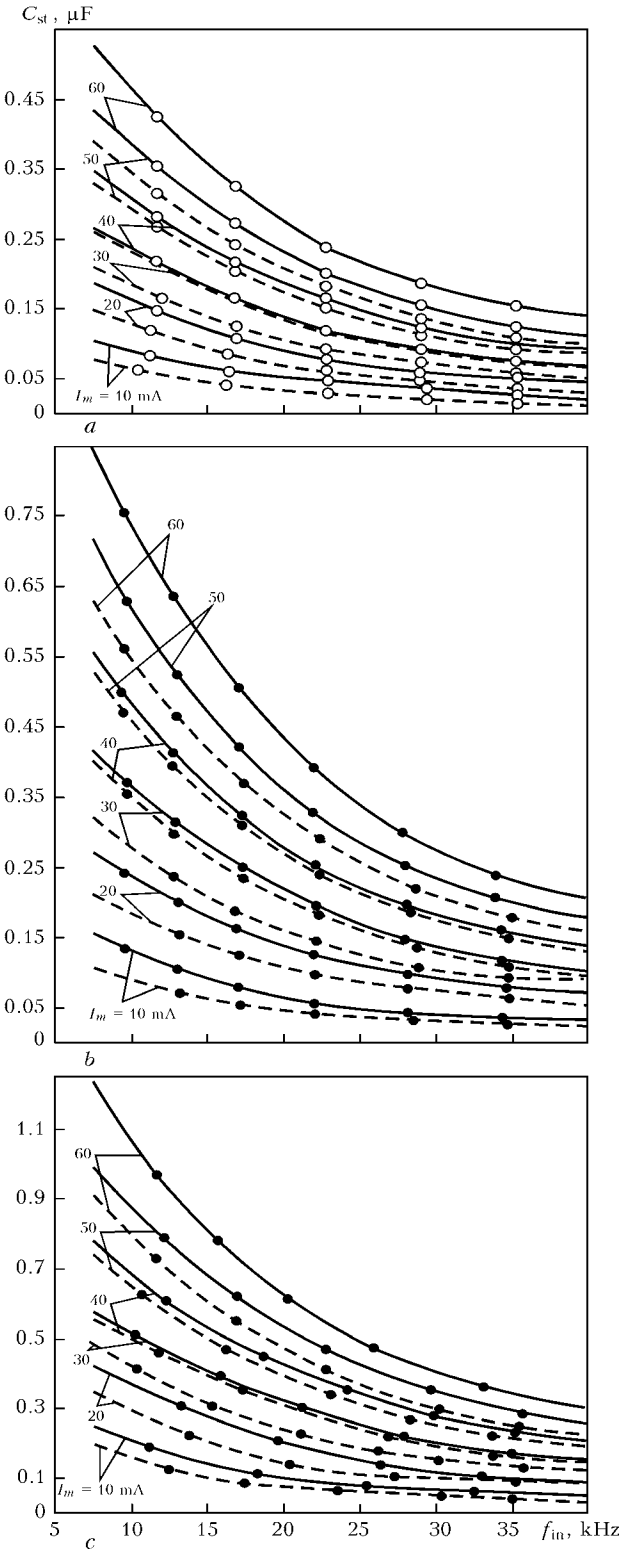

Figure 9. Dependence diagrams of $C_{st} = f(f_{in}, U_{in.m})$ capacity of each stage of VM at N = 3 (*a*), 4 (*b*) and 5 (*c*) and $U_{in.m}$ = 150 (*solid*) and 200 (*dashed curve*) V

1. Level of VM output voltage is selected, recommended values of which usually make $U_{out} = U_{C0} = (650 \pm 50)$ V.

2. Capacity C of GVP forming circuit, amount and specific type of capacitors forming this capacity (see Figure 6, $C5$) are determined using expression (14) and value, given in Table 1, as well as recommendations for CD based on key scheme with dosing reactor.

3. Number of multiplying stages N, amplitude of input voltage $U_{in.m}$ and maximum allowable voltage drop $\Delta U = k_s N U_{in.m}$ are determined considering that $U_{C0} = U_{out} = NU_{in.m} - \Delta U$ and using diagrams given in Figure 7. Assuming rational values of electric and weight-dimension parameters of VM, recommended values make:

$N = 4$, $U_{in.m} = 160–190$ V, $k_s = 0.07–0.10$. If circuit or structural peculiarities of welding inverter do not allow realizing recommended values of N and $U_{in.m}$, then their other values can be used with the help of given in Figure 7 dependence diagrams $\Delta U = f(U_{in})$ or expression

$$U_{out} = NU_{in.m}(1 - k_s). \quad (37)$$

4. Approximate value of capacitor capacity C_{st} of each VM stage are determined at recommended largest value of charge current I_m of GVP capacitive storage, being equal to 50–60 mA, assuming $N = 3 \div 5$, $U_{in.m} = 160–190$ V, $\Delta U = 0.1NU_{in.m}$ with the help of diagrams, given in Figure 8. If N or f_{in} values differ from indicated in Figure 8, then formulae (31) is used for value determination as well as data of Table 3, which provides for recommended values of I_m and R_{ch}, calculated considering their dependence on U_{out}, $T_{sw} = 1/f_{sw}$ values and capacity C of GVP forming circuit as well as expressions (14), (34) and (35) and values, indicated in Table 1.

5. C_{st} value is specified using diagrams given in Figure 9 at $N = 3 \div 5$ depending on input voltage frequency f_{in}, which makes 18–40 kHz in the most cases. Received values of capacity C_{st} (capacity of each of VM capacitors) are used for selection of the closest (with rounding to the largest side) value from 0.047, 0.068, 0.1, 0.15, 0.22, 0.33, 0.47, 0.68, 1.0 μF series, at that the largest allowable value of direct current U_{VDC} for all VM capacitors should fulfill $U_{VDC} \geq 2.2U_{in.m}$ condition. Metal-film capacitors with polypropylene or polyethylene dielectric, for example, MPR or PPN type or MER of HITANO Company are desirable.

6. I_m calculation value is specified by formulae (30) considering specific value of C_{st} and selected corresponding to it capacitor part-type. In the case when I_m values exceed recommended ones, VM capacitor part-type with larger capacity is selected.

7. Selection of VM diodes is carried out using such main parameters as allowable values of average direct current $I_{FAV\ max}$ and back voltage $U_{R\ max}$ as well as maximum values of forward voltage drop U_F and reverse recovery time t_{rr}. At that diode parameters should fulfill the conditions

$$I_{FAV\max} \geq 1.2I_{FAV}, \quad (38)$$

where I_{FAV} is the largest average value of direct current via diode, calculated on expressions (32) and (33) depending on form of input voltage, and

$$U_{R\max} \geq 2.2U_{in.m}, \quad (39)$$

as well as $U_F \leq 1.6$ V and $t_{rr} \leq 100$ ns.

VS-20ETF04FPPbF or VS-20ETF06FPPbF diodes of «Vishay Semiconductors» [20] or MURF1660CTG diode of «ON Semiconductor» companies [28] can be used, for example, in AESA VM according to combination of parameters and characteristics.

8. Formulae (36) is used for calculation of resistance of current-limiting resistor R_{lim} (see Figure 6, $R1$). The largest value of power dissipation $P_{R_{lim\ max}}$, emitted in R_{lim} resistor during first one-two cycles of charge of GVP capacitive storage, can be calculated by expression

$$P_{R_{lim\ max}} = (I_{C\ RMS})^2 R_{lim} = 0.25 I_m^2 R_{lim}, \quad (40)$$

where $I_{C\ RMS} = \sqrt{1/T_{sw} \int_0^{T_{sw}} i_C(t)^2 dt} = 0.5I_m$ is the root-mean-square (acting) value of charge current at approximation of exponential video pulse of charge current via video pulse of triangle form. Based on the fact that increase of $u_C(t)$ voltage on GVP capacitive storage provides for reduction of its charge current $i_C(t)$ and it equals zero up to the moment of charge end, then average value of power $P_{R_{lim}}$, emitted in resistor R_{lim} in course of charge duration of GVP capacitive storage, can be determined as

$$P_{R_{lim}} \approx 0.5 P_{R_{lim\ max}}. \quad (41)$$

If AESA is designed for stabilizing of burning of alternating arc, then minimum power $P_{R_{lim\ nom}}$ of resistor R_{lim} should be taken from condition

$$P_{R_{lim\ nom}} \geq 1.43 P_{R_{lim}}, \quad (42)$$

and if AESA is designed only for direct current arc excitation, then $P_{R_{lim\ nom}}$ value can be significantly reduced in comparison with calculation one and make 2–8 W.

C2-22-2 or C2-33-2 series resistors can be used as R_{lim} resistor at $P_{R_{lim}} \leq 3$ W, or SPS, SQZ, SQHG series [18] at $P_{R_{lim}} \geq 3$ W.

Conclusions

1. Application of VM-based CD is seemed to be sufficiently effective for AESA, imbedded in welding power sources, which include element of high-frequency transformation, and, respectively, high-frequency transformer. They are simple in realizing and have small values of weight-dimension and cost indices for such devices in comparison with other type CD. However, ap-

plication of CD based on VM is reasonable at AESA pulse energy levels do not exceeding 0.25 J, not more than 700 V of voltage charge of GVP capacitive storage and 150–200 V amplitude values of input voltage (AESA supply voltage) of 18–40 kHz frequency.

Peculiarity of CD based on VM lies in the fact that their functioning requires application of supply voltage of alternating current. At that, form of input voltage (AESA supply voltage) virtually has no effect on output characteristics and parameters of CD, however, significantly effects diode passing currents. Area of application of AESA with CD based on VM is limited by inverter power supplies, mainly for TIG welding.

2. CD based on key scheme with dosing reactor are inferior to CD based on VM in weight-dimension and cost characteristics, but, at the same time, have series of important advantages in comparison with the letter. CDs based on key scheme with dosing reactor do not depend on supply voltage type and can operate at supply voltage from direct as well as alternating current of sine- or rectangular-wave or close to this forms of frequency from tens of hertz (including 50 Hz) to tens of kilohertz. There are virtually no limitations for such CDs on level of input voltage, which can lie in the range of several to hundred of volts as well as on technically grounded levels of AESA pulse energy, which can make from 0.01 to 1 J and more, at that there is a possibility of stabilizing of set values of charge voltage of GVP capacitive storage. They have wide area of application in arc and plasma welding and can be used in traditional power supplies and welding systems and power supplies of inverter type. Such AESA can be efficiently used in manual arc and plasma methods and in automatic welding machines, in particular, single- and multi-station systems of automatic orbital TIG welding of pipeline joints [29].

3. Results of carried analysis and consideration of experience of development, designing, manufacture and operation of AESA allowed development of engineering procedure for calculation of CD based on key scheme with dosing reactor and CD based on VM as well as elaborating practical recommendations on selection of their element base, that can be useful not only for AESA development, but other similar devices, designed for application in different branches of science and technology.

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